UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/420,887	10/19/1999	PUTHIYA K. NIZAR	042390.P7149	3400

8791 7590 06/10/2003

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD, SEVENTH FLOOR
LOS ANGELES, CA 90025

EXAMINER
ROBERTSON, DAVID L

ART UNIT	PAPER NUMBER
2186	6

DATE MAILED: 06/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.

EXAMINER

ART UNIT	PAPER NUMBER
	6

DATE MAILED:

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☒ Responsive to communication(s) filed on March 24, 2003

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-23 is/are pending in the application.
Of the above, claim(s) _____ is/are withdrawn from consideration.
☐ Claim(s) _____ is/are allowed.
☒ Claim(s) 1-23 is/are rejected.
☐ Claim(s) _____ is/are objected to.
☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.
☐ The specification is objected to by the Examiner.
☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.
☐ received in Application No. (Series Code/Serial Number) _____.
☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of Reference Cited, PTO-892
☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____
☐ Interview Summary, PTO-413
☒ Notice of Draftperson's Patent Drawing Review, PTO-948
☐ Notice of Informal Patent Application, PTO-152

--SEE OFFICE ACTION ON THE FOLLOWING PAGES--

* U.S. GPO: 1998-404-498/40517

This Office action is in response to the Response and Declaration filed March 24, 2003.

Discussion Regarding the Declaration

Applicant's declaration under 37 C.F.R. § 1.131, attempting to swear behind the filing date of the prior art patent and publication is noted. However, § 1.131(1) states that prior invention may not be established under this section if:

> (1) The rejection is based upon a U.S. patent or U.S. PATENT application publication of a pending or patented application to another or others which claims the same patentable invention as defined in § 1.601(n).

The invention being claimed by applicants is the same as that claimed by Ryan in US 6,449,679 B2. The applications are claiming the same inventions as follows:

Ryan claim 14:

14. A processing system comprising:
a memory controller that issues and receives commands in a packet based RAMBUS DRAM protocol;
a plurality of memory modules each comprising column/row protocol based DRAM devices, the memory modules are located in in-line memory module sockets;
a single interface device located between the memory controller and the in-line memory module sockets, the interface device translates packet based RAMBUS DRAM protocol command and data signals from the memory controller into the column/row protocol, and the interface device translates data signals received from the memory modules into packet based RAMBUS DRAM protocol data.

Applicants' claim 20:

20. A memory subsystem comprising:
a memory control hub;
a memory channel coupled to the control hub;
a memory bus;
a memory device coupled to the memory bus; and
a memory translation hub coupled to the memory channel and to the memory bus, the memory translation hub to receive a memory control packet from the memory channel, and to generate memory control signals on the memory bus responsive to the memory control packet.

Ryan claim 23:

23. A method of operating a processing system comprising:
receiving packet based commands from a memory controller with a single interface device;
translating the packet based commands into column/row DRAM commands; and
communicating the column/row DRAM commands to a plurality of detachable memory modules.

Applicants' claim 17:

17. A method of connecting a memory bus to a memory controller hub through a memory channel comprising:
receiving a memory control packet from the memory channel;
translating the memory control packet to memory control signals; and
generating the memory control signals on the memory bus.

As can be seen above, the claims are clearly directed to the same patentable invention, though applicants' claims are slightly broader. Note that claim 14 of Ryan recites a "memory controller that issues...commands in a packet based RAMBUS DRAM protocol", this corresponds to the "memory control hub" of claim 20 of applicants, and to the "memory control packet from the memory channel." Similarly, the Ryan claim positively recites "column/row protocol based DRAM devices" which correspond to the "memory device coupled to the memory bus" in applicants' claims (see SDRAM DIMMs 104 in figures 1 and 2). The only other distinction is that Ryan additionally claims the translation and transmission of data along with the commands from the memory channel to the memory bus (i.e., Ryan, claim 14, lines 8-11, "the device translates packet based RAMBUS DRAM protocol command *and data signals* from the memory controller into the column/row protocol") and of data from the memory bus to the memory channel (i.e., Ryan, claim 14, lines 11-14, "and the interface device translates *data signals* received from the memory modules into packet based RAMBUS DRAM protocol data"), whereas applicants' independent claims recite the translation and transmission of the memory

control packet alone. Clearly, the translation and transmission of data, from the memory channel to the memory bus in the event of a write operation, and from the memory bus to the memory channel in the event of a read operation, are inherent and obvious with respect to applicants' claimed device (and specifically claimed in dependent claims 11-12, 15-16, 18-19 & 22-23).

Applicants' independent claim 20 has been discussed above. Applicants' other independent claims 1 and 13 do not positively recite the memory controller hub nor the memory device, however, these are clearly elements are claimed to be coupled to the "memory channel" and "memory bus", thus they are not patentably distinguishable. Of these claims, claim 13 is in means plus function form. Claim 13 reads:

> 13. A memory translation hub comprising:
> means for receiving a memory control packet from a memory channel;
> means for translating the memory control packet to memory control signals; and
> means for generating the memory control signals on a memory bus.

Regarding the "memory control packets" applicants' specification teaches:

> The MCH 120 provides a memory channel 122, such as a Rambus® channel, to support the memory channel architecture, such as the Direct Rambus™ architecture. Direct Rambus architecture provides a memory channel architecture that includes a physical channel structure, signaling levels, and a packet protocol. Direct Rambus™ architecture is further described in "Rambus® Technology Overview," DL-0040-00, Rambus Inc., February 12, 1999, which is incorporated by reference. (See page 7, lines 14-20).

Regarding the "memory control signals" and the "memory bus" applicants state:

> The protocol for controlling memory channel devices is also significantly different from the protocol for SDRAM. The memory channel protocol is based on packet communication between the MCH 120 and the memory channel devices 124. The protocol to control SDRAMs on DIMMs requires separate address and

> data lines and includes point to point control signals from the memory controller to device rows. The SDRAM architecture is further described in "JEDEC Standard No. 21-C, Release 4," which is incorporated by reference. (See page 8, lines 10-16.)

Thus, claims 1 and 13 are identical to the interface device of Ryan which translates packet based RAMBUS DRAM protocol commands from the memory controller into the SDRAM protocol of the attached memory devices.

Applicants' dependent claims 2-10, 14-16 and 21 are directed to the physical structure of the RAMBUS memory channel, which is well known, and further, is identical to the RAMBUS structure disclosed by Ryan (see Ryan, figure 3). Claims 11-12, 15-16 and 22-23 are directed to the translation and transmission of data, either from the one bus (e.g., the memory channel) to the other (e.g., the memory bus), or vice versa; which is expressly recited in claim 14 of Ryan. Claims 2-10 further recite features that are believed to be an integral part of the prior art Direct Rambus™ architecture as described in the "Rambus® Technology Overview," DL-0040-00 referred to by applicants, and thus it would have been obvious to include these limitations, if for no other reason than to maintain compatibility with memory controllers that implement the Direct Rambus™ architecture as described in "Rambus® Technology Overview," DL-0040-00.

With respect to method claims 17-19, the "packet based commands" of Ryan correspond to the "memory control packet" of applicants, Ryan names the source, "from a memory controller" while applicants name the path, "from the memory channel." It is clear that in both cases, the memory translation hub is connected to "a memory controller" through a "memory

channel" (see claim 17 preamble). The "column/row DRAM commands" of Ryan correspond to the "memory control signals" of applicants. Again, Ryan names the destination, "a plurality of detachable memory modules" while applicants name the path, "on the memory bus." As before, in both cases, the "memory bus" connects to "detachable memory modules." Finally, claims 18-19 are directed to the movement of data back and forth.

Therefore, because applicants are claiming the same invention as Ryan, prior invention may not be established under 37 C.F.R. § 1.131. Furthermore, the merits of the Declaration have not been considered.

Invitation to Copy Claims

The following allowable claim is suggested for the purpose of an interference:

A processing system comprising:
a memory controller that issues and receives commands in a packet based RDRAM protocol;
a plurality of memory modules comprising SDRAM devices; and
a single interface device located with the memory controller such that the interface device is not located on the memory modules, the interface device translates packet based RDRAM protocol command and data signals from the memory controller into an SDRAM protocol, and the interface device translates data signals received from the memory module into packet based RDRAM protocol data.

The suggested claim must be copied exactly, although other claims may be proposed under 37 CFR 1.605(a).

Applicants should make the suggested claim within ONE MONTH or THIRTY DAYS from the mailing date of this letter, whichever is longer. Failure to do so will be considered a

disclaimer of the subject matter of this claim under the provisions of 37 CFR 1.605(a). THE PROVISIONS OF 37 CFR 1.136(a) DO NOT APPLY TO THIS TIME PERIOD.

Claims 1-23 are considered unpatentable over this suggested claim.

Rejection of Claims 1-23

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for the purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English Language;

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-23 are rejected under 35 U.S.C. 102(e) as being anticipated by either Ryan (US 2001/0042163 A1) or Ryan (US 6,449,679 B2). The particulars can be found in the discussion regarding the claims, above, and in the previous Office action. Because of the reasons noted above, applicants' Declaration has not been considered.

Claims 1-23 are rejected under 35 U.S.C. 102(a) as being anticipated by "SDRAM to Direct RDRAM" (hereafter the *presentation*). The presentation teaches a memory translation hub (I/F Chip) that includes an interface that is connected to RAMBUS memory channel (see RIMM Sockets) through which it receives a memory control packet and includes at least one memory bus interface connected to SDRAM chips. Clearly the I/F Chip receives commands and/or data from the Memory Controller (see figure) in the form of memory control packets and data packets and causes appropriate SDRAM commands and data to be sent to the SDRAM chips, and conversely will receive data from the SDRAM chips in SDRAM protocol and will send corresponding data packets to the memory controller. Note that the RIMM socket inherently includes and supports all of the physical and protocol features that are found on a conforming Direct RDRAM channel.

Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ingenio *et al.* (US 6,041,361). The Ingenio reference teaches a translation device (see memory control device 108, figures 1, 2a or 2b) which is designed to translate one form of memory commands received from a memory controller (104) over a bus or channel corresponding to the first protocol (see synchronous interface 106); the translation device translating the commands into a format

appropriate for the connected memory devices (see memory devices 110, 112) via an appropriate bus (not numbered), so that a second form of memory may be attached directly to the memory control device without requiring a change in the system memory controller (see column 4, lines 55-57). While the main portion of the specification is described where the system memory controller natively supports only a subset of SDRAM protocol and teaches a translating memory control device so that any industry standard SDRAM may be connected thereto, the reference specifically states that the invention also applies to connecting an SDRAM compatible system memory controller to RAMBUS® memory (see column 6, lines 41-50). In this event, the communication between the memory control device would clearly correspond to all of the pertinent RAMBUS® requirements and protocols. The reference does not teach or suggest connecting a RAMBUS® compatible system memory controller to SDRAM memory. However, the general teaching of the reference, which is not obscured by the particular examples given, is that busses and protocols from a system memory controller supporting one type of memory may be made to be compatible with memory requiring otherwise different busses and protocols by use of a suitable intervening memory control device which translates and converts the one to the other. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified the input and output interfaces of the memory control device taught by Ingenio to accommodate any system memory controller/memory device combination desired or required, as the need arose, thus applicant's invention was obvious. Note that it goes without saying that the claimed

particulars of the RAMBUS® protocol would clearly have been included by one of ordinary skill in any such translation device coupled to a RAMBUS® type system memory controller, including the specific limitations of claims 2-12, 14-16, 18-19 and 21-23. Additionally, the concept of returning data from a connected memory device to the particular system memory controller follows inherently, including the specific limitations of claims 11-12, 14-16, 18-19 and 21-23. Thus the claims are not patentable.

Conclusion

Applicants' arguments filed March 24, 2003 have been fully considered but they are not persuasive for the reasons set forth above.

Applicants need not respond to the remaining issues in this action if a suggested claim is copied for the purpose of an interference within the time limit specified above (37 CFR 1.605(b)).

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 746-7239, (for formal communications to Technology Center 2100 intended for entry)

Or:

(703) 746-7240 (for informal or draft communications to Technology Center 2100, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

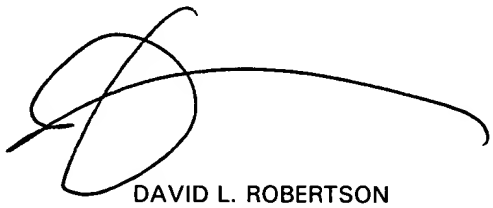
Any inquiry of a general nature or relating to the status of this application should be directed to the technology center receptionist whose telephone number is **(703) 305-3900**.

Direct any inquiries concerning drawing review to the Drawing Review Branch (703) 305-8404.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L. Robertson whose telephone number is (703) 305-3825.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached at 305-3821. **The fax number for Technology Center 2100 for Official communications is (703) 746-7239.**

Communications which are not application specific may also be posted on e-mail at *David.Robertson@USPTO.gov*.



DAVID L. ROBERTSON
PRIMARY EXAMINER
ART UNIT 2186

C:\DOCS\WPWIN61\03ACT\420887R2.WPD
June 5, 2003

Attachment for PTO-948 (Rev. 03/01, or earlier)
6/18/01

The below text replaces the pre-printed text under the heading, "Information on How to Effect Drawing Changes," on the back of the PTO-948 (Rev. 03/01, or earlier) form.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

1. Correction of Informalities -- 37 CFR 1.85

New corrected drawings must be filed with the changes incorporated therein Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not been assigned to the application. If this information is provided, it must be placed on the front of each sheet and centered within the top margin. If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings **MUST** be filed within the **THREE MONTH** shortened statutory period set for reply in the Notice of Allowability. Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136(a) or (b) for filing the corrected drawings after the mailing of a Notice of Allowability. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

2. Corrections other than Informalities Noted by Draftsperson on form PTO-948.

All changes to the drawings, other than informalities noted by the Draftsperson. **MUST** be made in the same manner as above except that, normally, a highlighted (preferably red ink) sketch of the changes to be incorporated into the new drawings **MUST** be approved by the examiner before the application will be allowed. No changes will be permitted to be made, other than correction of informalities, unless the examiner has approved the proposed changes

Timing of Corrections

Applicant is required to submit the drawing corrections within the time period set in the attached Office communication. See 37 CFR 1.85(a).

Failure to take corrective action within the set period will result in **ABANDONMENT** of the application.